FEATURES

1. **ROM:**
   - RISC 2T core
   - 4K x 16 bits MTP
1. **EEPROM: 256 x 8 bits**
2. **RAM: 256 x 8 bits**
3. **STACK: 8 Levels**
4. **System Clock type selections:**
   - Fast clock from 1~20 MHz Crystal (FXT)
   - Fast clock from Internal RC (FIRC, 16 MHz)
   - Slow clock from 32768 Hz Crystal (SXT)
   - Slow clock from Internal RC (SIRC, 65.5 KHz+-2%@25℃/V_{CC}=5V)
5. **System Clock Prescaler:**
   - System Clock can be divided by 1/2/4/8 option
6. **Power Saving Operation Mode**
   - FAST Mode: Slow-clock is enabled, Fast-clock keeps CPU running
   - SLOW Mode: Fast-clock can be disabled or enabled, Slow-clock keeps CPU running
   - IDLE Mode: Fast-clock and CPU stop. Slow-clock, T2, or Wake-up Timer keep running
   - STOP Mode: All clocks stop, T2 and Wake-up Timer stop
7. **3 Independent Timers**
   - Timer0
     - 8-bit timer divided by 1~256 pre-scale option / auto-reload / counter / interrupt / stop function
   - Timer1
     - 8-bit timer divided by 1~256 pre-scale option / auto-reload / interrupt / stop function
     - Overflow and Toggle out
   - T2
     - 15-bit timer with 4 interrupt interval time options
     - IDLE mode wake-up timer or used as one simple 15-bit time base
     - Clock source: Slow-clock, Fsys/128, or FIRC/512 (16 MHz/512)
8. **Interrupt**
   - Three External Interrupt pins
     - 1 pin is falling edge wake-up triggered & Interrupts
     - 2 pins are rising or falling edge wake-up triggered & Interrupt
   - Timer0 / Timer1 / T2 / Wake-up Timer Interrupt
   - ADC Interrupt
   - Comparator Interrupt

- PWM Interrupt
- LVD Interrupt
- All Port Pin Change Wakeup Interrupt
- EEPROM Interrupt

9. Wake-up Timer (WKT)

- Clocked by built-in RC oscillator with 4 adjustable interrupt times
  - 15.6 ms / 31.3 ms / 62.5 ms / 125 ms @V_{CC}=5V

10. Watchdog Timer (WDT)

- Clocked by built-in RC oscillator with 4 adjustable reset times
  - 125 ms / 250 ms / 1001 ms /2001 ms @V_{CC}=5V
- Watchdog timer can be disabled / enabled in STOP mode

11. Six 16 bits PWMs

- Six individual duty-adjustable, shared period-adjustable
- PWM clock source: System clock (Fsys), FIRC/256, FIRC (16 MHz), FIRC*2 (32 MHz)
- PWM0 supports complementary output (PWM0P, PWM0N)
- PWM0 output with dead-zone(non-overlap) time durations adjustable: (0~15)*(PWMCLK)
- PWM0N/0P/1/2/3/4/5 has two outputs
- Half-bridge phase control output

12. 12-bit ADC with 14 channels for External Pin Input and 2 channels for Internal Voltage

- Two internal voltage channels: VBG, 1/4VCC
- ADC reference voltage: V_{CC}, V_{BG} (1.2V), V_{BG} (2.48V) and V_{BG} (2V)
- PWM trigger ADC

13. Comparator

- Comparator x 1
  - With 7-bit DAC input
  - DAC reference voltage: V_{CC} or V_{BG} (1.20V or 2.48V)

14. Reset Sources

- Power On Reset
- Watchdog Timer Reset
- Low Voltage Reset
- External Pin Reset

15. Low Voltage Reset (LVR) and Low Voltage Detection (LVD)

- 15-Level Low Voltage Reset: 1.73V ~ 3.5V, can be disabled
- 15-Level Low Voltage Detection: 1.73V ~ 3.5V, can be disabled

16. Operating Voltage

- Fsys= 16 MHz, PWMCKS=FIRC*1, LVR~5.5V. Suggest LVR ≥ 2.30V
- Fsys= 8 MHz, PWMCKS=FIRC*1, LVR~5.5V. Suggest LVR ≥ 1.6V

Note: Refer to the "Electrical Characteristics Graphs".

17. **Operating Temperature Range : -40°C to + 105°C**
18. **Table Read Instruction: 16-bit ROM data lookup table**
19. **Integrated 16-bit Cyclic Redundancy Check (CRC) function**
20. **Instruction set: 39 Instructions**
21. **I/O ports:**
    - Maximum 18 programmable I/O pins
      - Open-Drain Output
      - CMOS Push-Pull Output
      - Schmitt Trigger Input with pull-up ／ pull-down resistor option(PA7 has no pull-down resistor)
      - All I/O with High-Sink except PA7
      - 1/2 V_{CC} (LCD 1/2 bias) Output (except PA7)
    - All pin change wake up (falling edge and rising edge trigger) and interrupt
22. **LCD Driver**
    - Maximum 17 software controlled COM
    - LCD 1/2 bias
23. **Programming connectivity support 5-wire (ICP) or 6-wire program**
24. **RDCTL: Read signal delay control for Program ROM**
    - **The user must switch this register to "4ns" to enhance the performance of minimal operating voltage**
25. **Trimmed VBG1.2V/2V**
    - The users could move BG2TRIM to BGTRIM for exact 2V VBG.
26. **ATD: Automatic transient detection(Read signal length control for Program ROM) to enhance the performance of power consumption at slow mode**
27. **Package Types:**
    - 20-pin SOP (300 mil)
    - 16-pin SOP (150 mil)
    - 14-pin SOP (150 mil)
    - 8-pin SOP (150 mil)
    - 20-pin TSSOP (173 mil)

PIN ASSIGNMENT DIAGRAM