FEATURES

1. **ROM:**
   - RISC 2T core
   - 2K x 16 bits MTP
2. **RAM: 128 x 8 bits**
3. **EEPROM: 256x 8 bits，endurance 1million write cycle**
4. **STACK: 8 Levels**
5. **System Clock type selections:**
   - Fast clock from Internal RC (FIRC, 16 MHz)
   - Slow clock from Internal RC (SIRC, 93 KHz@V_{CC}=5V)
6. **System Clock Prescaler:**
   - System Clock can be divided by 1/2/4/8 option
7. **Power Saving Operation Mode**
   - FAST Mode: Slow-clock is enabled, Fast-clock keeps CPU running
   - SLOW Mode: Fast-clock can be disabled or enabled, Slow-clock keeps CPU running
   - IDLE Mode: Fast-clock and CPU stop. Slow-clock or Wake-up Timer keep running
   - STOP Mode: All clocks stop, Wake-up Timer stop
8. **2 Independent Timers**
   - Timer0
     - 8-bit timer divided by 1~256 pre-scale option / auto-reload / counter / interrupt / stop function
   - Timer1
     - 8-bit timer divided by 1~256 pre-scale option / auto-reload / interrupt / stop function
     - Overflow and Toggle out
9. **Interrupt**
   - Three External Interrupt pins
     - 1 pin is falling edge wake-up triggered & Interrupts
     - 2 pins are rising or falling edge wake-up triggered & Interrupt
   - Timer0 / Timer1 / Wake-up Timer Interrupt
   - ADC Interrupt
   - PWM Interrupt
   - LVD Interrupt
   - All Port Pin Change Wakeup Interrupts
10. **Wake-up Timer (WKT)**
    - Clocked by built-in RC oscillator with 4 adjustable interrupt times
      - 11 ms / 23 ms / 46 ms / 91 ms @V_{CC}=5V
11. **Watchdog Timer (WDT)**

- Clocked by built-in RC oscillator with 4 adjustable reset times
  - 91 ms / 183 ms / 732 ms / 1463 ms @V_{CC}=5V
- Watchdog timer can be disabled / enabled in STOP mode

12. Six 16 bits PWMs

- Six individual duty-adjustable, shared period-adjustable
- PWM clock source: System clock (Fsys), FIRC/256, FIRC (16 MHz), FIRC*2 (32 MHz)
- PWM0 supports complementary output (PWM0P, PWM0N)
- PWM0 output with non-overlap time durations adjustable: (0~15)*(PWMCLK)
- PWM0N/0P/1/2/3/5 has only one output

13. 12-bit ADC with 13 channels for External Pin Input and 2 channels for Internal Voltage

- Two internal voltage channels: VBG, 1/4VCC
- ADC reference voltage: V_{CC}, V_{BG} (1.2V), V_{BG} (2.48V) and V_{BG} (2V)

14. Reset Sources

- Power On Reset
- Watchdog Timer Reset
- Low Voltage Reset
- External Pin Reset

15. Low Voltage Reset (LVR) and Low Voltage Detection (LVD)

- 15-Level Low Voltage Reset: 1.73V ~ 3.5V, can be disabled
- 15-Level Low Voltage Detection: 1.73V ~ 3.5V, can be disabled

16. Operating Voltage

- Fsys= 16 MHz, LVR~5.5V. Suggest LVR ≥ 2.30V
- Fsys= 8 MHz, PWMCKS=FIRC*1, LVR~5.5V. Suggest LVR ≥ 1.55V

Note: Refer to the "Electrical Characteristics Graphs".

17. Operating Temperature Range : -40°C to + 105°C

18. Table Read Instruction: 16-bit ROM data lookup table

19. Integrated 16-bit Cyclic Redundancy Check (CRC) function

20. Instruction set: 39 Instructions

21. I/O ports:

- Maximum 14 programmable I/O pins
  - Open-Drain Output
  - CMOS Push-Pull Output
  - Schmitt Trigger Input with pull-up resistor option
  - All I/O with High-Sink except PA7
- All pin change wake up (falling edge and rising edge trigger) and interrupt

22. Programming connectivity support 5-wire (ICP) or 7-wire program

23. RDCTL: Read signal delay control for Program ROM

- **The user must switch this register to "4ns" to enhance the performance of minimal operating voltage.**

24. **Trimmed VBG1.2V/2V**
    - The users could move BG2TRIM to BGTRIM for exact 2V VBG.
25. **ATD: Automatic transient detection to enhance the performance of power consumption at slow mode**
26. **Package Types:**
    - 8-pin SOP (150 mil)

PIN ASSIGNMENT DIAGRAM

PA6 -- EEPROM SDA
PB0 -- EEPROM SCL